High Performance Organic Nonvolatile Flash Memory Transistors with High-Resolution Reduced Graphene Oxide Patterns as a Floating Gate

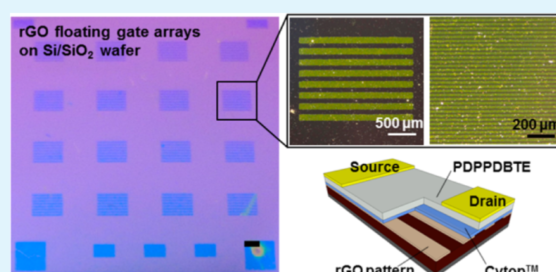
Dae Sung Chung,*,† Sung Min Lee,† Jang Yeol Back,§ Soon-Ki Kwon,§ Yun-Hi Kim,*,‡ and Suk Tai Chang*,†

†School of Chemical Engineering and Materials Science, Chung-Ang University, Seoul 156-756, Republic of Korea

‡Department of Chemistry and RINS, Gyeongsang National University, Jinju 660-701, Republic of Korea

§School of Materials Science and Engineering and ERI, Gyeongsang National University, Jinju, 660-701, Korea

ABSTRACT: High-performance organic nonvolatile memory transistors (ONVMTs) are demonstrated, the construction of which is based on novel integration of a highly conductive polymer as a semiconductor layer, hydroxyl-free polymer as a tunneling dielectric layer, and high-resolution reduced graphene oxide (rGO) patterns as a floating gate. Finely patterned rGO, with a line width of 20−120 μm, was embedded between SiO_2 and the polymer dielectric layer, which functions as a nearly isolated charge-trapping center. The resulting ONVMTs demonstrated ideal memory behavior, and the transfer characteristics promptly responded to writing and erasing the gate bias. In particular, the retention time of written/erased states tended to increase as the rGO line width was reduced, implying that the line width is a critical factor in suppressing charge release from rGO. Using a 20-μm-wide rGO pattern, a nonvolatile large memory window (>20 V) was retained for more than 5×10^5 s, which is 50 times longer than non-patterned rGO films.



KEYWORDS: *organic devices, nonvolatile memory devices, reduced graphene oxide, thin films, micropatterning, charge-trapping layers*

■ INTRODUCTION

Electrically reprogrammable and preferably nonvolatile memory devices based on organic materials have continued to grow over the past decade because of their distinct advantages, such as solution processability, light-weight, low cost, and the possibility of being integrated with printed electronics on a plastic substrate.[1−10] Organic memory devices can be categorized into various types according to their operating mechanisms, such as resistive switching devices,[2,3] ferroelectric dielectric devices,[6,7] and floating gate devices.[8,9] Among these, floating gate devices, which are operated by capacitance modulation of the trapping sites in the floating gate, are particularly attractive because their memory characteristics can be easily tuned by strategically selecting and/or engineering the trapping sites. In such organic nonvolatile memory transistors (ONVMTs), metallic nanoparticles are one of the most frequently used trapping sites because of their quantum-confined characteristics, which considerably reduce the possibility of charge loss from a nanoparticle to the underlying dielectric layer.[10] A limiting factor, owing to the use of nanoparticles as a floating gate, is the relatively narrow memory window due to the inherent band gap restriction.[11]

Graphene oxide (GO) can be another floating gate candidate because oxidized GO domain has a wide band-gap that can act as an effective charge trapping site.[13] In fact, GO sheets have been successfully integrated into inorganic[13] and even organic[12] memory devices as charge-trapping layers, resulting in non-volatile large memory windows. Recently, a reduced graphene oxide (rGO) layer partially covering a 3-aminopropyltriethoxysilane (APTES) treated substrate was used as a charge-trapping layer in a nonvolatile memory device.[14] Although further investigations are required to understand the charge trapping effect of rGO flakes, their structural defects and residual oxygen functional groups are considered to act like charge trapping sites in memory devices.[14,15] Nonetheless, earlier reports have mainly focused on the use of GO or rGO sheets as charge trapping centers for increasing the memory window. Thus far, there have been no attempts to confine these charge-trapping centers to enhance the nonvolatile properties of memory devices.

With that in mind, we show that line-patterned rGO (with fine line width) can be much better charge trapping centers for ONVMTs without compromising the large memory window in nonvolatile memory operations. Novel ONVMTs are fabricated using a highly conductive polymer as the semiconductor layer, hydroxyl-free polymer as the tunneling dielectric layer, and patterned rGO thin film as the floating gate. In this study, we have used highly stable polymeric semiconductors, i.e., poly[2,5-bis(2-octyldodecyl)pyrrolo[3,4-*c*]pyrrole-1,4(2H,5H)-dione-(*E*)-1,2-di(2,2′-bithiophen-5-yl)ethene] (PDPPDBTE),

Received: March 28, 2014
Accepted: May 20, 2014
Published: May 20, 2014

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as well as a hydroxyl-free polymer dielectric, i.e., Cytop. These elements together allow a threshold voltage (V_{th}) shift that originates only from the rGO because the trapping sites in semiconductors have a negligible effect even after air/electrical exposure.[16] Following the analysis of transfer characteristics under repeated writing and erasing gate bias, we demonstrate large threshold voltage shits (Memory window >15 V). More importantly, we show that the memory retention time of ONVMTs with line-patterned rGO thin films tends to increase as the line width of patterned rGO decreases, thereby resulting in a retention time greater than 5×10^5 s when a 20-μm line pattern was used.

EXPERIMENTAL SECTION

Preparation of rGO Thin Film. An aqueous GO solution produced by the Hummers method[17] was obtained from Graphene Supermarket (New York, U.S.A.). The GO dispersion was centrifuged at 8000 rpm for 10 min to remove unexfoliated flakes (WiseSpin CF-10, Daihan Scientific), followed by mixing with ultrapure Milli-Q water to obtain a GO solution with a concentration of 2.4 mg mL^{-1}. Uniform rGO thin films on Si/SiO_2 substrates were prepared using the meniscus-dragging deposition (MDD) technique.[18] Briefly, a glass microscope slide (25×75 mm^2 with plain end, Fisher Scientific) and Si/SiO_2 wafer, which are used as a deposition plate and coating substrate, respectively, were hydrophilized with a piranha solution for 30 min and rinsed with DI water. Once the deposition plate was in contact with the coating substrate at an angle of 30°, a 40-μL drop of GO solution was injected between the two plates. The deposition plate was pushed in place with an alternating motion generated by a motorized stage (AL1-1515-3S, Micro Motion Technology) with a constant speed of 20 mm s^{-1}. The deposition was repeated 20 times (one alternating back-and-forth motion is defined as one deposition). The resulting GO films was reduced using hydriodic (HI) acid vapor at 80 °C for 3 h, yielding thin rGO films.

Formation of rGO Patterns. An Si wafer was coated with SU-8 25 photoresist (MicroChem, Inc.) to a thickness of 20 μm using a spin-coater (ACE-200, Spin Coater). A photo mask containing line-pattern printouts was placed onto the SU-8 photoresist layer and was exposed to UV light (UVCURE-60PH, Lichtzen). The UV-exposed photoresist was treated in SU-8 developer solution (MicroChem, Inc.). Polydimethylsiloxane (PDMS) prepolymer (Sylgard 184, Dow Corning) was cast onto the photoresist master to prepare the pre-patterned elastomeric molds used for patterning the rGO films. After curing them at 70 °C for 6 h, the PDMS molds were peeled off from the master. The rGO film and the pre-patterned PDMS mold were exposed to air plasma (PDC-32G, Harrick Plasma) for 20 s at a power of 6.8 W and for 90 s at 18 W, respectively, before being brought into contact with each other for several minutes. After removing the PDMS molds, high-resolution rGO line-patterns were formed on the Si/SiO_2 substrates.

Device Fabrication. ONVMTs were fabricated on a common gate of highly n-doped silicon with a 100-nm thick, thermally grown SiO_2 dielectric layer. After the rGO patterns were treated with UV ozone for 10−20 min, a thin layer of Cytop (Asahi Glass) was spin-coated onto the SiO_2 dielectric layer (~20 nm). A solution containing PDPPDBTE was spin-coated at 2000 rpm from 0.7 wt % chloroform solutions to form thin films with nominal thickness of 50 nm, as confirmed by the surface profiler (Alpha Step 500, Tencor). The films were annealed at 200 °C for 10 min under a nitrogen atmosphere. Gold source and drain electrodes were evaporated on top of the semiconductor layers (60 nm). For all constructions, typical channel widths (W) and lengths (L) were 1600 and 160 μm, respectively.

Characterization. Optical images of the rGO patterns were acquired by an Olympus BX-51 optical microscope mounted on a high-resolution ProRes CF Scan digital CCD camera (Jenoptik). The thickness of the rGO patterns was measured using an atomic force microscope (AFM) (XE-100, psia). The electrical characteristics of the fabricated devices were measured in air using Keithley 236 and Keithley 2400 source/measure units combined with a home-built LabVIEW program. Gate bias signals at various frequencies were supplied by an arbitrary signal generator (AFG310, Tektronix), and the source-drain responses were recorded using either the LabVIEW program or a digital phosphor oscilloscope (TDS 5052, Tektronix) depending on the time scale.

RESULTS AND DISCUSSION

Figure 1 shows the procedures followed to prepare the line-patterned rGO floating gate for ONVMTs by applying the plasma-enhanced detachment patterning (PEDP) method.[19] This method begins with coating a uniform rGO thin film onto a hydrophilized Si/SiO_2 substrate using the MDD. Separately, a PDMS mold, containing stripe-shaped micropatterns, is prepared. Both the rGO film and PDMS mold are then exposed to oxygen plasma and subsequently brought into conformal contact without any additional pressure or heating. The exposure to oxygen plasma improves the work of adhesion between the rGO and PDMS surfaces by enhancing the surface polarity of both surfaces without significant damage to the rGO thin films at the relatively low power plasma condition used in this study.[19,20] Adhesion of such strength between the two surfaces can give a rise to selective detachment of the rGO film from the substrate, while peeling off the pre-patterned PDMS mold. The inset in Figure 1c shows the arrays of a line-patterned rGO on the Si/SiO_2 surface. Figure 2a−c shows the typical types of patterned rGO floating gates used in this study: film type, 120-μm-wide stripes, and 20-μm-wide stripes, respectively. The floating gates have uniform thickness of about 7 nm, as shown in Figure 2d. The as-prepared rGO floating gates used in the manufacturing of ONVMTs were assembled with thin layers of Cytop and PDPPDBTE conducting polymer, as shown in Figure 1d.

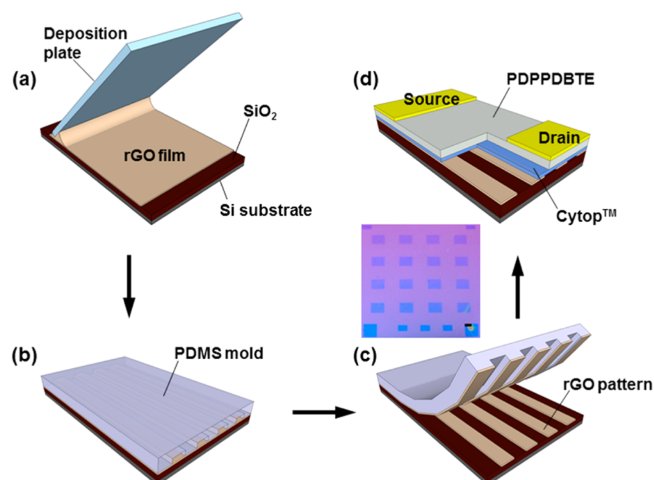

Figure 1. Schematic illustration of line-pattern fabrication for a rGO film. (a) Fabrication of rGO thin film on Si/SiO_2 substrate using the MDD technique. (b) Oxygen plasma treatment of pre-patterned PDMS mold and rGO film, and conformal contact between the two surfaces. (c) Removal of the PDMS mold. (d) ONVMT device with high-resolution rGO line-patterns. The inset of (c) shows the optical micrograph of line-patterned rGO arrays. The scale bar in the inset image is 1 mm.

The fabricated ONVMTs with various types of rGO (non-patterned GO film, line-patterned rGO) displayed typical memory behaviors, as shown in Figure 3. The transfer characteristics (drain-source current vs gate voltage) of the

dx.doi.org/10.1021/am501909v | ACS Appl. Mater. Interfaces 2014, 6, 9524−9529

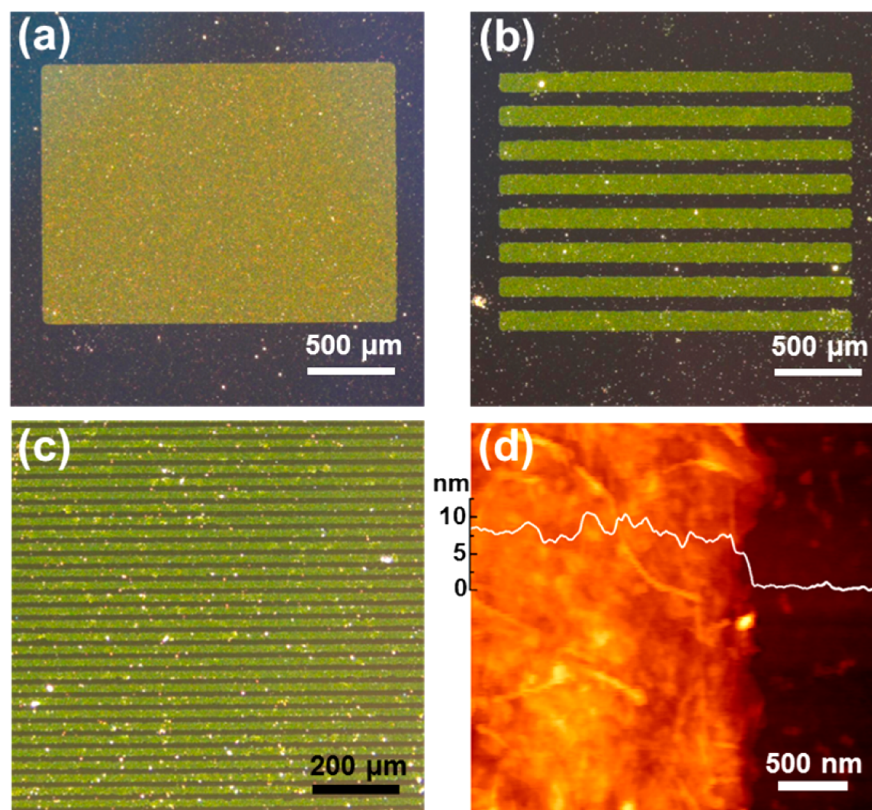

Figure 2. Optical microscope images of floating gate layers in ONVMTs. (a) rGO thin film and line-patterned rGO with width of (b) 120 μm and (c) 20 μm. (d) AFM image of the line-patterned rGO on a Si/SiO_2 substrate with a height profile.

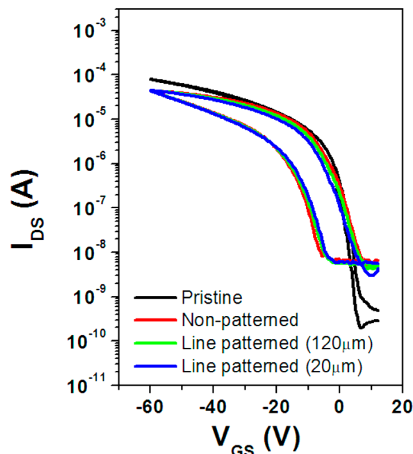

Figure 3. Transfer characteristics of the various transistors used in this study. Both the forward and backward sweeps are included to illustrate the hysteresis windows of the devices.

ONVMTs without rGO, with non-patterned rGO film, and with line-patterned (20 μm and 120 μm) rGO are summarized after measuring under both forward and reverse gate sweeps. All the devices revealed reasonably high charge carrier mobility of 0.2−0.3 $cm^2/(V\ s)$. The observed low hysteresis for the rGO-free device and large hysteresis window (~20 V for non-patterned and ~15 V for line-patterned) for rGO-devices indicate the effective charge trapping ability of rGO. The larger hysteresis window of ONVMTs with non-patterned rGO, compared to that with line-patterned rGO, can be attributed to the larger effective area of the rGO being exposed to the upper deposited polymeric semiconductor. Note that line-patterned rGO has ~40% smaller effective area than the non-patterned film, as shown in Figure 2a−c.

The performance of ONVMTs, used as electrically programmable and erasable memory devices, was evaluated by applying gate voltage pulses of fixed duration and measuring the corresponding transfer characteristics. In contrast to Si-flash memory devices, which operate with n-type MOSFETs, the written state of p-type ONVMTs, (where p-type polymeric semiconductors are used) corresponds to the moment when enough hole-charge carriers are stored in the rGO (floating gate), resulting in a negative shift in the threshold voltage (V_{th}). Conversely, the erased state can be defined as the moment when trapped hole charge carriers are flushed out of the rGOs, restoring V_{th} to its original value. Figure 4a−c shows that the transfer functions of ONVMTs with non-patterned rGO film and line-patterned rGO were substantially shifted in the negative direction after applying a gate bias of −60 V. Reverse control of these transfer functions was also possible by applying a positive gate bias of 60 V. Furthermore, these memory characteristics were quite robust and reproducible. As shown in Figure 4d−f, during the 20 writing/erasing cycles, ONVMTs maintained memory windows of 27, 24, and 18 V for non-patterned rGO, 120- and 20-μm-wide line-patterned rGO, respectively. The magnitude of programming voltage also has an effect on memory performance. For small gate bias of up to 10 V, the transfer characteristics remained nearly unchanged. Once the gate bias reach a critical value of ~15 V, however, the shift in V_{th} becomes significant. This result is a very encouraging one because the negligible shift in V_{th} at low programming voltage allows non-destructive read-out for flash memory applications. It is also notable that reasonable memory

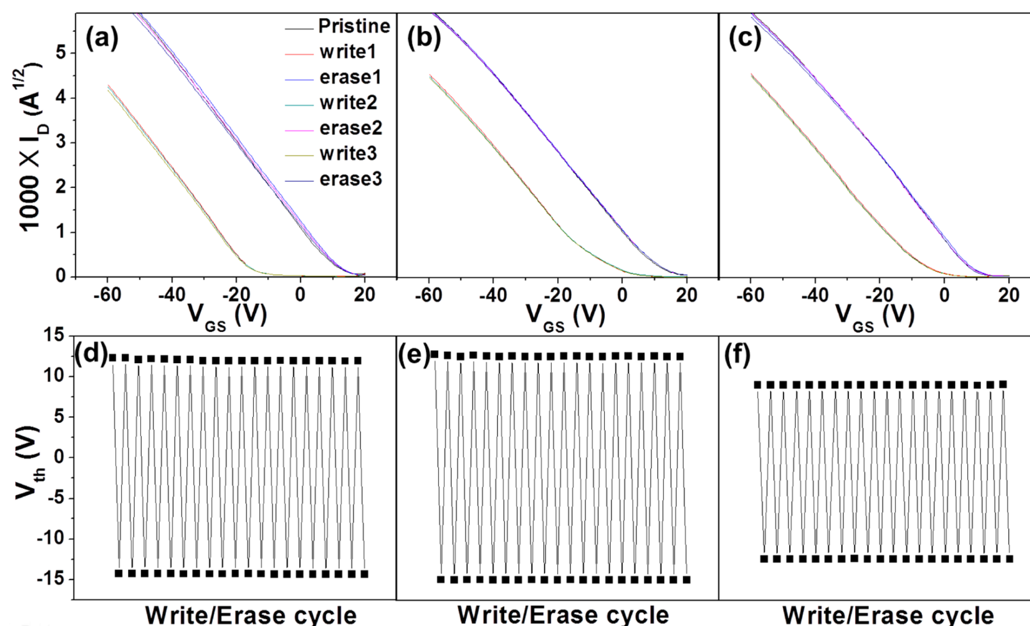

Figure 4. (a)−(c) Transfer characteristic states of ONVMTs in a write/erase cycle of (a) non-patterned, (b) 120-μm-wide line-patterned, and (c) 120-μm-wide line-patterned rGOs. (d),(e) V_{th} as a result of repeated write/erase cycles with the same sequence as in the upper panel.

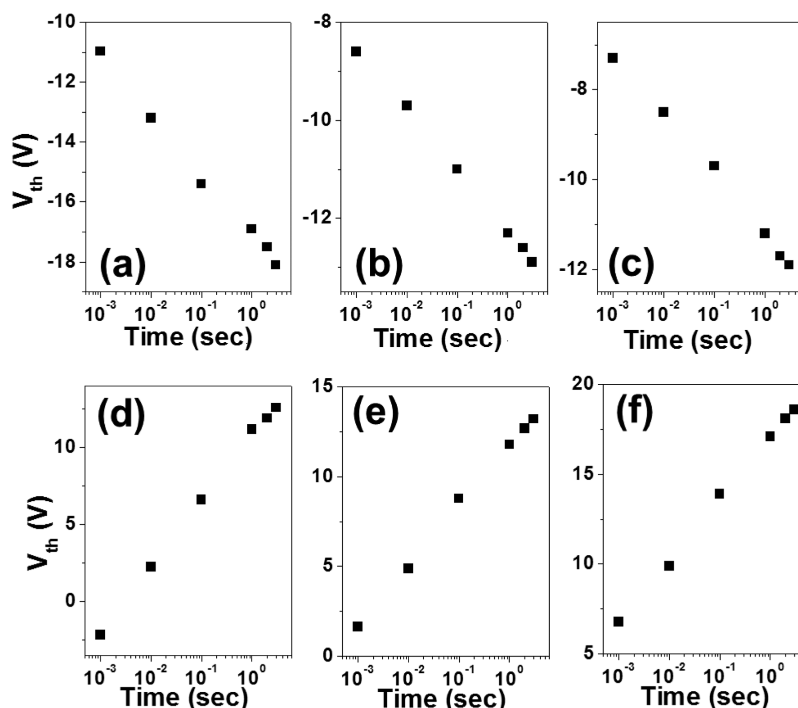

Figure 5. V_{th} as a function of (upper panel) writing and (lower panel) erasing voltage. (From left to right in each panel: non-patterned, 120-μm-wide line-patterned, and 20 μm-wide line-patterned rGO floating gates).

windows were obtained at low gate voltage (∼20 V) owing to the thin polymeric tunneling layer.

The trapping mechanism of the charge carriers was further characterized by investigating the shift of V_{th} as a function of programming time. The change in V_{th} is monitored while the write/erase time is increased, and the gate bias is kept constant at ±60 V. In Si-flash memory transistors, incremental changes to the threshold voltage can be attributed to the time (t) dependence of the stored charge,[21] i.e.,

$$\Delta V_{th}(t) = -Q(t)/C$$

where Q and C are the total charge and capacitance of the dielectric layer, respectively. It is well known that regardless of the assumption of trap distribution or tunneling probability, charge trapping models predict a logarithmic time dependence of total charge[22] as follows:

$$Q \approx \ln(t/t_0)$$

Figure 5a−f shows the logarithmic dependence of V_{th} on time under writing and erasing, respectively. Together with the above-mentioned theoretical description, these results support

that the memory operation of our ONVMT follows that of conventional Si-flash memory devices. Having trapped holes in rGO, which is a consequence of applying a negative gate bias, means that fewer holes are injected from the source to the channel during the transfer sweep (writing). Trapped holes are then released by applying a positive gate bias, thus no longer inhibiting hole injection from the source to the channel (erasing).

For nonvolatile memory applications, excellent retention ability is a key figure of merit. To investigate this behavior, the following measurements were conducted. After applying a writing gate bias (−60 V) under the conditions stated in Figure 3, the shifted V_{th} was monitored as a function of time. Between the various measurement points, the device was kept in the dark without being exposed to electrical stress. As shown in Figure 6, in all the devices, V_{th} was conserved for nearly 10^4 s,

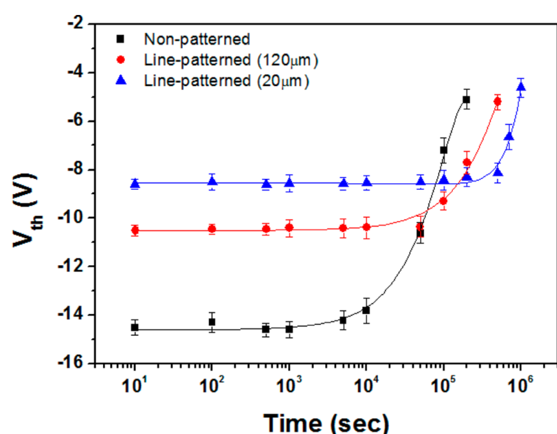

Figure 6. Retention time of various ONVMTs with non-patterned, 120-μm-wide line-patterned, and 20 μm-wide line-patterned rGO floating gates.

thereby implying slow relaxation of trapped charge carriers from rGO. After 10^4 s, V_{th} of ONVMT with non-patterned rGO films started to display a rather drastic positive shift. Interestingly, however, ONVMT with line-patterned rGO revealed a much longer retention time of up to 10^5 s. Surprisingly, ONVMTs with a narrower line width (20 μm) exhibited an even longer retention time, of up to 5×10^5 s. One possible explanation for this is their discrete nature compared to non-patterned rGO films. The stored charge in a line-patterned rGO is in fact isolated, and any minor damage on a dielectric layer does not significantly affect the total stored amount of charge. Actually, this is the most important reason why small-sized nanoparticles with discrete nature are practically used for the floating gate of nonvolatile memory transistor.[11,24,25] The enhancement of retention using a narrower line pattern supports this agreement. Other reports with non-isolated graphene film and graphene oxide film yielded the rather shorter retention time of 10^3~10^4 s.[12,23,27] In addition, in those earlier results,[12] which report the first ONVMT with GO as a floating gate, a rather thick tunneling dielectric layer was used to fully prevent the trapped charges from being released, which resulted in a retention time of 10^4 s. However, it is worthwhile to note that such a thick tunneling layer not only improves the retention behavior, but also increases the programming voltage. In our results, we combine a thin tunneling layer (Cytop ~20 nm) that allows a low programming voltage down to 20 V, and a patterned rGO that enables a long retention time up to 5×10^5 s. To the best of our knowledge, this is the first report on the long duration electrical stability of rGO-based organic memory devices achieved by strategic engineering of rGO. For comparison, other organic non-volatile memory devices that employed Au nanoparticles as a floating gate yielded retention times ranging from 10^3 to 10^5 s.[27−30]

CONCLUSIONS

In summary, we have demonstrated high-performance organic nonvolatile memory transistors (ONVMTs) by introducing a high-resolution line-patterned rGO as an effective floating gate. The resulting rGO-based ONVMTs exhibits superior retention time as well as transfer characteristics that respond promptly to writing and erasing gate bias, compared to other graphene-based memory devices. The improvements are primarily attributed to the nearly isolated charge-trapping center of the finely patterned rGO. The patterning method described here is easy and scalable to large-area rGO floating gate arrays on rigid or flexible substrates. Thus, this technology can potentially play a key role in future electronic memory devices.

AUTHOR INFORMATION

Corresponding Authors

*E-mail: dchung@cau.ac.kr.
*E-mail: ykim@gnu.ac.kr.
*E-mail: stchang@cau.ac.kr.

Notes

The authors declare no competing financial interest.

ACKNOWLEDGMENTS

This Research was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIP) (2012047047) and Basic Science Research Program through the National Research Foundation of Korea (NRF) funded by the Ministry of Education (NRF-2013R1A1A2012177).

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